REMARKS/ARGUMENTS

Remarks regarding Specification

Examiner has requested that Applicant update information cited under "Cross-Reference to Related Applications" in page 1 of the original specification. That section is currently accurate, in describing the priority claimed to a prior provisional application. If Examiner wishes to relate this application to some other application Examiner deems related, Applicant respectfully requests that more specific details be provided.

Examiner has remarked that lines 8-9 at page 24 comprise a claim without a claim number. That issue has been rectified in the amended claims submitted herewith by deleting the aforementioned text and adding new Claim 25.

Remarks regarding Claims amendments:

As a preliminary matter, and responsive to Examiner's second comment under paragraph 1 "Specification" of the Office Action, Applicant has deleted the limitation referenced, and has added new Claim 25 which includes the limitation as a dependent claim.

With reference to Examiner's Claim Objections:

- Claims 1, 4, 6, 7, 12, 14, 15, 17 and 22 are rewritten to replace "co-efficient" with "coefficient;
- Claim 8 already reads as Examiner has requested, without amendment (please advise if this is not so in Examiner's records). This appears to be a printing error in the published application, but was not an error in Applicant's originally filed application;
- Claim 15 (as mentioned above) is rewritten to replace "co-efficient" with "coefficient; and
- Claim 20 already reads as Examiner has requested, without amendment (please advise if this is not so in Examiner's records). This appears to be a printing error in the published application, but was not an error in Applicant's originally filed application;

and Applicant submits that the foregoing corrects the Claims to overcome the Examiner's Claim Objections.

To clarify, a significant differentiating feature of Applicant's invention, claims 1, 12, 15 and 21 have been amended to include a step-counter provided with each butterfly unit to

which the unit's selectable multiplier is responsive. This finds support in Figures 11 and 12 at Sn, and paragraphs 0045 (where the switch is controlled by a control signal, which is provided by an adder (which is implements a step-counter for that butterfly unit) read with the switch's control of the selectable multiplier(s) in paragraph 0047 (by way of example). Specifically, Claim 1 has had added "the selection being responsive to a step-counter of each butterfly" after the words: "…on output sequences of adjacent butterfly modules," at line 5; similarly, claim 22 has been amended by adding the words: "responsive to a step-counter with the butterfly unit" before the words: "…selectively multiplying the generated 2-point FFT sequence…" at line 7 thereof.

Applicant has modified claims 1, 12, 15 and 21 to include specific reference to the triplets as processor modules acting on data inputs and with data outputs to more clearly state Applicant's claim as having physical components acting on and producing tangible results.

Applicant represents that no new matter is added by these amendments. Applicant requests that the application be amended as above described.

Remarks and Argument with respect to s.101

Examiner has rejected claims 1-24 (new 1-25) as being directed to non-statutory subject-matter, stating that the processor cites the transformation of an input sequence according to a mathematical algorithm. With respect, Applicant points out that the processor claimed is described in the Specification as a triplet based FFT processor that allows for a physical implementation in a reduced semiconductor area due to a reduction in the hardware complexity in comparison to numerous systems of the prior art (paragraph 0025). The pipelined processor claimed thus not only provides for transformation of an input data sequence, but does so in a novel concrete and tangible way which produces efficiencies due to reduced hardware complexity.

Additionally, the data input sequence being subjected to the FFT in the processor's function is described in the specification as a digital signal or series of digitized signal samples (e.g. paragraphs 0018, 0039) accomplished in a VLSI chip (e.g. paragraphs 0027, 0042).

Applicant respectfully submits that the amended processor and method claims (being the processing of digital input being sequenced samples) and the resulting advantages described (being the reduction of semiconductor area due to decreased hardware complexity)

provide a concrete, useful and tangible result and overcome Examiner's objection of non-statutory subject-matter.

Applicant submits that these arguments overcome Examiner's rejection of non-statutory subject-matter under s.101, and that, in this regard at least, the application, as amended, is fit for allowance.

Remarks and Argument with respect to s.102

Examiner (in paragraph 6) has rejected each of Applicant's claims in light of Yeh (US 2004/0059766). With respect, applicant submits that the Yeh reference is substantially different and distinguishable from the present invention, and thus does not engage the application of s.102.

Yeh discloses a central control unit (claim 1, 4th and 5th subparagraphs; also paragraph 0009, paragraph 0011, 606 at figure 10, 706 at figure 12, and 806 at figure 13) which controls each BFI, BFII and BFIII. (see also 36 at figure 3). Yeh's control unit also issues the required coefficients centrally (806b at figure 13; also paragraph 0076). Significantly, Applicant's invention includes local control units (using a step counter) in each BF unit, and provides coefficient tables in each BF unit. Applicant's explanation follows:

This invention does not use Yeh's form of global "centralized" control for at least the following reasons:

1. Applicant's invention would have immunity to the duty cycle of the data coming in to the FFT. In Applicant's invention, each butterfly section makes its own control decision as to what can be done at any time, while the Yeh "centralized" solution would have to halt the machine if there were any gaps in timing of provision of any input.
2. Applicant designed the FFT to be fully pipelined, that is, Applicant's invention can send another signal sample in to the FFT directly after the last sample of a previous FFT operation has been passed to the FFT. This then permits 2 different FFT operations to be working in the FFT unit at the same time. With distributed control provided in the invention of Applicants' application this is easy to do, but is more difficult in Yeh's centralized control system, chiefly due

to co-ordination and timing problems requiring further control systems and hardware.

3. Applicant provides an implementation that is immune to latency changes of any butterfly element within the FFT. It is often the case that the pipeline depth of the core is altered to meet different timing requirements for ASIC or FPGA implementation. In the distributed control system of Applicants' invention, the output signal is just delayed appropriately to match data latency. No other block in the system is required to have information about any delay that has occurred earlier in the processing. However, for Yeh's (or anyone's) centralized control scheme, each new pipelining arrangement will require a new central controller that must be adapted to provide control signals at the correct times to each butterfly element in the FFT.
4. Applicant's invention also uses a distributed table of coefficients to locally provide twiddle factors to the complex multipliers. This provides each node with locally connected coefficient tables that only contain values needed at that node. Yeh seems to use a single table to serve coefficients to all complex multipliers from a central location (para 0076 and figure 13 806b). A central coefficient table would mean that each multiplier would have to have a separate read port at the memory (ROM area would grow linearly with each added port) or the control unit would have to stall one operation in favor of another, increasing control complexity and increasing latency. A central ROM coefficient table also suffers from significant routing difficulties, all this getting worse as the size of the FFT increases (Applicant uses 1024 or even 2048 point FFTs).

Applicant respectfully submits that, despite the similarity of certain of the steps or functions in Yeh, Applicant's invention provides for a significantly different and improved decentralized or atomic control mechanism/function and as well an improved decentralized coefficient providing system in an FFT processor, which Yeh is not seen to disclose or suggest. These things, it is submitted, are sufficient to distinguish Applicant's invention from Yeh's in a novel and non-obvious way.

In particular, Yeh's claim 1 includes a single "centralized" control unit which controls each BFI, each BFII and each BFIII and provides each coefficient according to a value held in a single pipeline step-count register. Applicant's invention provides a step-counter at each BF unit (see Figures 11 and 12, at Sn and Sn-12), providing a control signal to a switch onboard each BF unit, clearly showing atomic or decentralized control units, one for each BF unit of the system. This difference is true with respect to all of the embodiments disclosed in Yeh. Applicant has attempted to clarify this differentiating feature in certain of the claim amendments detailed above.

With respect, applicant submits that, with the amendments to the claims set forth herein, and in light of the clarification and argument made above, the application, as amended, is fit for allowance.

Respectfully submitted,
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